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VOLTAGE DIVIDERS

How a voltage divider splits a voltage, why it sags under load, and how to scale a higher voltage into an ADC. With a live calculator.

ONE THOUSAND DRONES ENGINEERING TEAM · VERIFIED 2026-07

A voltage divider is two resistors in series that split a voltage. The output, tapped between them, is a fixed fraction of the input set by the two resistor values.

$$Vout = Vin \times R2 / (R1 + R2)$$

CALCULATOR · VOLTAGE DIVIDER CALCULATOR (VOUT, R1, R2)

Compute a resistive divider's output voltage and quiescent current from Vin, R1, and R2. Sized for fitting a higher voltage into an ESP32's 3.3 V ADC.

Interactive calculator: academy.onethousanddrones.com/tools/voltage-divider

COMPUTE A DIVIDER'S OUTPUT AND THE CURRENT IT DRAWS.

WHY IT SAGS UNDER LOAD

The divider only holds its ratio while almost nothing draws current from the tap. Connect a real load and it pulls the output down, because the load acts like a third resistor. So a divider suits a high-impedance input that draws almost no current, and it is a poor way to power anything.

SCALING A VOLTAGE INTO AN ADC

An ESP32-S3 analog input reads roughly 0 to 3100 mV with its highest attenuation, near the `3.3 V` rail (Espressif ESP-IDF). To read a higher voltage, say a battery above the rail, a divider scales it down into that range so the ADC can measure it safely. The ADC pin draws almost no current, which is exactly the light load a divider needs.

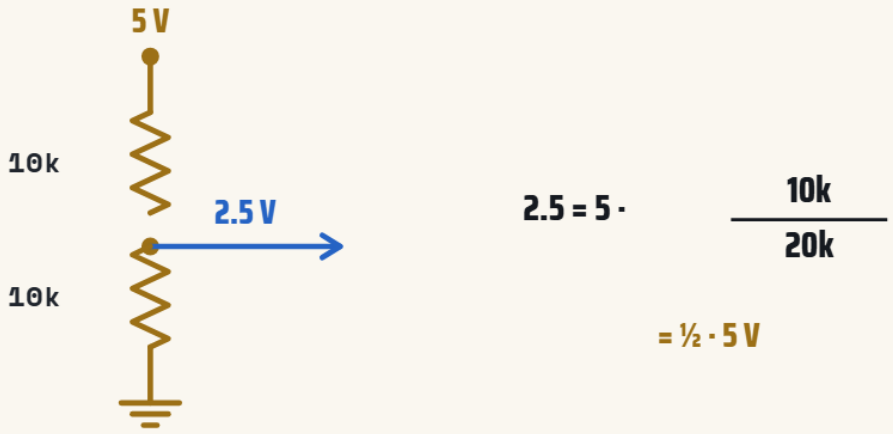
- Espressif. ESP-IDF Programming Guide: ESP32-S3 Analog to Digital Converter (ADC), input range and attenuation.- docs.espressif.com

DEEP DIVE · CLEANING UP THE READING IN FIRMWARE

Real resistors carry a tolerance and the ADC itself has an offset, so the raw number a divider hands the chip is close, not exact. Two cheap firmware habits close the gap. First, average: read the pin several times in a row and take the mean, and the random jitter shrinks. Second, calibrate: measure the known error once against a trusted meter, store it as a fixed offset, and subtract it from every future reading. The hardware sets the ballpark, and a few lines of firmware make it accurate. Espressif's ESP-IDF ships an ADC calibration API for exactly this.

▸ FUNDAMENTALS · VOLTAGE DIVIDER

VOLTAGE DIVIDERS



Vout = Vin × R2 / (R1 + R2). Two equal resistors halve the input: 5 V taps out at 2.5 V.

THE OUTPUT IS A FIXED FRACTION OF THE INPUT, SET BY R1 AND R2.

CHECKPOINT

1. A voltage divider's output is what?

a. Always half the input

b. A fixed fraction of the input set by the two resistors

c. The same as the input

ANSWER · B

Vout = Vin x R2 / (R1 + R2); the ratio depends on the resistor values.

2. What happens when you draw significant current from a divider's output?

a. The output rises

b. Nothing changes

c. The output sags below its no-load value

ANSWER · C

The load acts like a third resistor and pulls the output down, so dividers suit high-impedance inputs.

3. A voltage divider is a good way to do what?

a. Scale a voltage into an ADC's input range

b. Power a motor from a higher rail

c. Store energy for later

ANSWER · A

Its light-load fraction is ideal for a high-impedance ADC input, not for powering a load.

- Prerequisite: resistors
- Calculate it: the voltage divider calculator
- Next: capacitors and decoupling