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FROM SCHEMATIC TO BOARD: THE LAYOUT WORKFLOW

The fixed sequence that turns a schematic into a real PCB: assign footprints, import the netlist, place, route, run DRC, and export the fab files. In KiCad terms.

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A finished schematic is half a design. The other half is the physical board, and the path between them is a fixed sequence: capture the schematic, give every part a footprint, push the netlist into the PCB editor, place the parts, route the copper, run the design-rule check, and export the fab files. Learn that sequence once and every board you draw follows it.

THE TWO FILES SHARE ONE NETLIST

A KiCad project holds two linked documents: the schematic and the PCB. You do not redraw one into the other by hand. They share a netlist, the machine-readable list of which pins connect to which. You draw the circuit once in the schematic, and `Update PCB from Schematic` carries that netlist into the board so the two can never silently disagree (KiCad).

- KiCad. PCB Editor (Pcbnew) documentation: Update PCB from Schematic, placement, routing, DRC, and fabrication outputs.- docs.kicad.org

A FOOTPRINT FOR EVERY SYMBOL

Each schematic symbol is an abstract part. Before it can live on a board it needs a footprint, the real copper-and-hole pattern it solders to. Assigning footprints ties the symbol to a physical part and to its bill-of-materials line, so `U2` on the schematic becomes one `SOT-23-5` land pattern on the board. A symbol with no footprint cannot be placed.

THE NETLIST IS THE CONTRACT

The netlist is what the PCB editor trusts. Every connection you drew, and only those, show up as a ratsnest: thin lines between the pads that still need copper. If a wire is missing on the schematic it is missing here too, so you fix the circuit in the schematic and re-import, never by drawing a stray trace on the board.

> **RUN ERC BEFORE YOU LEAVE THE SCHEMATIC**
> The electrical-rule check reads the schematic for unconnected pins, conflicting outputs, and power nets with no source. Clearing it before you import the netlist means the board you place is built on a circuit that already checks out, so a layout problem stays a layout problem and not a hidden schematic bug.

THE WORKFLOW IS FIXED: SCHEMATIC TO NETLIST TO PLACEMENT TO ROUTING TO DRC TO FAB FILES.

THEN PLACE, ROUTE, CHECK, EXPORT

With the netlist imported you place the footprints, route copper to satisfy the ratsnest, run the design-rule check against your fabricator's limits, and plot the gerbers. Each of those is its own guide in this cluster. What matters first is the shape of the whole: schematic, netlist, placement, routing, DRC, fab files, in that order, every time.

CHECKPOINT

1. What ties a schematic symbol to a physical part on the board?

a. Its footprint assignment

b. Its color on the schematic

c. The order it was drawn

ANSWER · A

A footprint is the real land pattern the symbol solders to; assigning it links symbol, part, and BOM line.

2. How does the circuit you drew get into the PCB editor?

a. You redraw it by hand on the board

b. It is emailed to the fabricator

c. The shared netlist is imported with `Update PCB from Schematic`

ANSWER · C

The schematic and PCB share a netlist; importing it keeps the two in sync.

3. You find a missing connection while routing. Where do you fix it?

a. Draw a new trace on the board only

b. In the schematic, then re-import the netlist

c. In the exported gerber files

ANSWER · B

The schematic owns the netlist; fix the circuit there and update the PCB so the two never disagree.

- Prerequisite: reading a schematic
- See it on a real board: the L1.01 build
- Next: footprints and land patterns