LIBRARY · REFERENCE GUIDE

DESIGN RULES AND DRC

The design-rule check is the board's spell-check. Set the rules to your fabricator's capabilities and clear every clearance, width, hole, and short before you leave the layout.

ONE THOUSAND DRONES ENGINEERING TEAM · VERIFIED 2026-07

The design-rule check is the board's spell-check. It compares your layout against a set of manufacturing limits, the clearances, trace widths, and hole sizes, and flags every place the board breaks them. Set the rules to your fabricator's capabilities, and do not leave the layout until the check is clean.

WHAT THE RULES COVER

The core rules are geometric: the minimum clearance between two pieces of copper, the minimum trace width, the minimum drilled hole, and the minimum annular ring (the collar of copper around a via or pad). Each is a number your fabricator can hold. Set them tighter than the fab and boards come back wrong; set them looser and you waste some space, but the board still builds.

MATCH THE RULES TO YOUR FAB

Every fabricator publishes a capability sheet: the smallest trace, space, hole, and ring they reliably make. You copy those numbers into the design rules before you route, so the check enforces what your chosen fab can actually build. A board that passes against the wrong fab's limits can still fail in production.

THE CHECK CATCHES MORE THAN GEOMETRY

DRC also finds electrical mistakes the layout introduced: two nets shorted by overlapping copper, a connection in the netlist with no trace yet (an unrouted net), and courtyards that overlap because two parts sit too close. KiCad reports each as a marker you jump to and fix (KiCad).

- KiCad. PCB Editor (Pcbnew) documentation: the design rules and the Design Rules Check (DRC). docs.kicad.org

> **A CLEAN DRC IS A HARD GATE**
>
> The courses here treat `DRC = 0` the way they treat `ERC = 0` on the schematic: a hard gate you clear before the board is allowed to move forward. An unrouted net or a clearance violation that ships is a board that does not work or cannot be built. Clear every marker, then export.

DRC FLAGS WHAT THE FAB CANNOT MAKE: CLEARANCE VIOLATIONS, UNROUTED NETS, AND SILK OVER PADS.

DEEP DIVE · ANNULAR RING AND WHY IT FAILS

The annular ring is the ring of copper left around a drilled hole after the drill bites. If a via's ring is too thin and the drill wanders even slightly, the hole breaks out of the pad and the connection is unreliable. Fabs quote a minimum annular ring and the DRC enforces it, because this is one of the quiet ways a cheap board fails: it passes a glance but the plating barely catches the pad. Give vias a ring with margin over the fab minimum.

CHECKPOINT

1. What should you set the design rules to match?

a. The largest board you have made

b. The schematic's net count

c. Your chosen fabricator's capabilities

ANSWER · C

Copy the fab's capability sheet into the rules so DRC enforces what they can build.

2. An unrouted net flagged by DRC means what?

a. A connection in the netlist has no copper trace yet

b. The board is physically too large

c. A part is drawn in the wrong color

ANSWER · A

DRC checks the layout against the netlist and flags connections still missing copper.

3. In the course gate model, `DRC = 0` is treated as what?

a. An optional cleanup at the end

b. A hard gate you clear before moving forward

c. A cosmetic preference

ANSWER · B

Like ERC on the schematic, a clean DRC gates the board; every marker is fixed before export.

- Prerequisite: PCB stackups
- See it on a real board: the L1.01 build
- Next: silkscreen, soldermask, and polarity marks